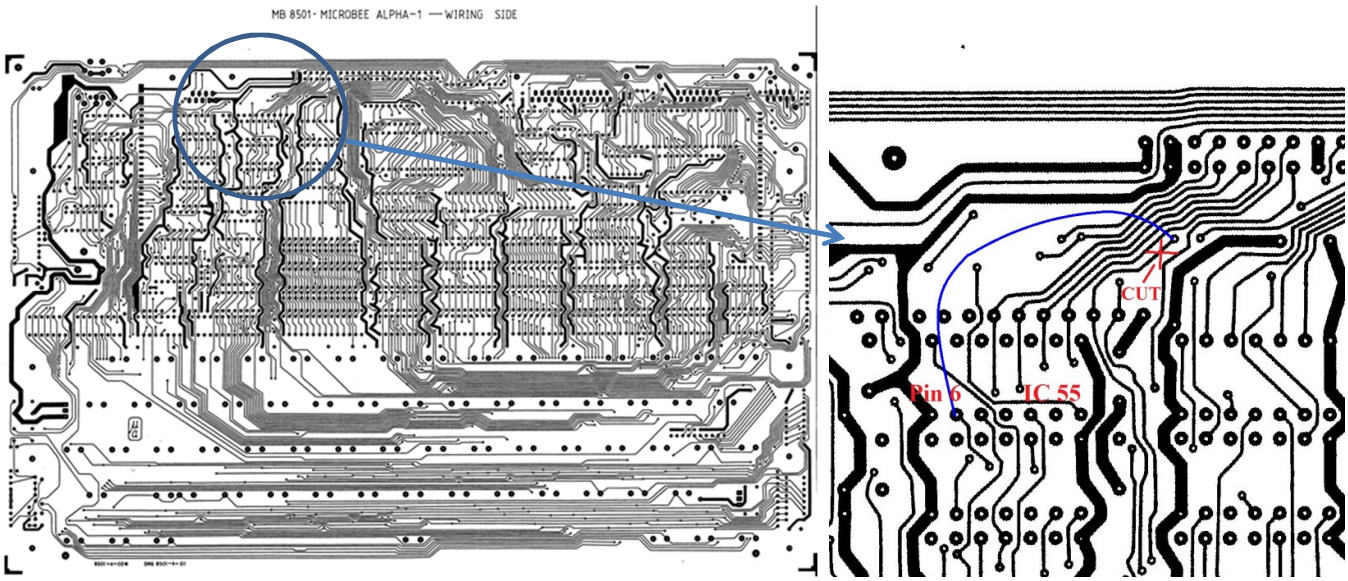
Microbee Technology Pty Ltd

Engineering Change Order
#20120714-2

ECO to be applied to product : Premium Plus Kit Computer
Part or sub-assembly: Baseboard PCB
PCB part #: 8501-4

Background:
Accesses to the screen section of ram (Screen, Attribute, Color & PCG rams) by the Coldfire processor on the Premium Plus coreboard have to be synchronised to non “screen refresh” times. Normally, when operating in Z80 mode, the screen control circuitry issues a WAIT signal to the processor until a valid access period is available at which time the WAIT signal is negated & the processor can complete its bus cycle (read or write access).
The Coldfire MCF52259’s external bus interface does not have any way to hold off the completion of a bus cycle however, so special synchronisation logic had to be implemented in the gate array to ensure screen memory accesses would happen at the correct time.
To achieve this, the MUX signal from the video circuitry had to be brought up to the gate array on the coreboard. This MUX signal, when high, signifies access to the screen memory is now available.
To facilitate the availability of the MUX signal on the coreboard the WAIT signal allocated on connector X7 (25 was socket strip) of the baseboard has been removed and this pin is now used to carry the MUX signal up to the gate array.

Fitting of ECO:



Start by cutting the track as shown in the diagram which runs from Pin 3 of RN3 to a via (drawings show underside of board where track cut is to be made). Solder Solder a wire line (using wire wrap wire or similar) between the via of the cut track to Pin 6 of IC55.

For Premium Plus kit serial numbers less than #PP0017, a software patch will be required to update the gate array logic image that is stored in the internal flash memory of the Coldfire processor on the coreboard. If the kit serial number is #PP0017 or above, the patch / update will have already been applied during manufacture & testing of the coreboard.